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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,295	FOTLAND ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-15 and 18* is/are allowed.

6)☐ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *16 and 17* is/are objected to.

8)☒ Claim(s) *18-27* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/11/04, 11/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS filed 12/14/04 and 7/14/05*.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 19-27 are directed to inventions that are independent or distinct from the invention originally claimed for the following reasons:

I. Claims 1-18 are drawn to an arithmetic operation, classified in class 712, subclass 221.

II. Claims 19 and 20 are drawn to a single-bit semaphore system using masks, classified in class 712, subclass 224.

III. Claims 21-23 are drawn to accessing and rearranging bytes of data, classified in class 712, subclass 300.

IV. Claims 24-27 are drawn to instruction modification, classified in class 712, subclass 226.

2. Inventions I, II, III, and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as masking values to set and clear a semaphore, invention III has separate utility such as accessing data across boundaries of 32-bit words with a register while avoiding partial register writes, invention IV has separate utility such as instruction modification based on the condition of an instruction. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and the search required for Groups II, III, and IV are not required for Group I, restriction for examination purposes as indicated is proper.

4. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 19-27 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 3, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, 1995 (herein after Intel), in view of Case et al., US Patent 4,777,587.

7. Intel has taught a method for performing arithmetic in a memory to memory architecture in an embedded processor, the method comprising:

a. receiving an instruction (Intel, page 25-29) specifying a source address in a memory (Intel, page 25-29 and 25-11, r/m8, r/m16, r/m32), a source address in the register file (Intel, page 25-29 and 25-10, r8, r16, r32), a destination address in the memory (Intel, page 25-29 and 25-11, r/m8, r/m16, r/m32), and a mathematical operation to be performed (Intel, page 25-29, ADD instruction); and

b. responsive to receiving the instruction:

c. accessing, from the source address in the memory, a first operand on which the mathematical operation is to be performed (Intel, page 25-29 and 25-11, r/m8, r/m16,

r/m32);

d. accessing, from the source address in the register file, a second operand on which the mathematical operation is to be performed (Intel, page 25-29 and 25-10, r8, r16, r32);

e. performing the mathematical operation on the first operand and the second operand to obtain the result (Intel, page 25-29, ADD instruction); and

f. storing the result in the destination address in the memory (Intel, page 25-29 and 25-11, r/m8, r/m16, r/m32).

8. Intel has not specifically taught that the instruction is a fixed length instruction. Case et al. have taught that using fixed length instructions, or RISC (reduced instruction set computers) instructions, enables the instructions to be easily decoded (Case et al., column 1, lines 15-17). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions of Intel be of a fixed-length, as taught by Case et al., for the desirable purpose of simplifying instruction decoding (Case et al., column 1, lines 15-17).

9. Intel may not have specifically taught the following:

a. the fixed length instruction is a 32-bit fixed length instruction,

b. specifying the source address in a memory using 11 bits, a source address in the register file using 5 bits, a destination address in the memory using 11 bits, and a mathematical operation to be performed using 5 bits.

10. However, it as been held that change in size is not a patentable difference, *In re Rose, 105 USPQ 237 (CCPA 1955)*. Any length of the fixed-length instructions and any length of the claimed specifiers are not patentably distinct over the prior art.

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to have:

a. the fixed-length instruction be any number of bits, including 32 bits,

b. specifying the source address in a memory using any number of bits, including 11 bits, specifying a source address in the register file using an number of bits, including 5 bits, specifying a destination address in the memory using any number of bits, including 11 bits, and specifying a mathematical operation to be performed using any number of bits, including 5 bits,

12. as it has been held that changes in size is not a patentable difference *In re Rose, 105 USPQ 237 (CCPA 1955).*

13. The rejection is respectfully maintained and incorporated by reference as set forth in the last office action, mailed on June 1, 2004.

14. Referring to claims 2 and 3, Intel and Case have taught the method of claim 1, as described above. They have not specifically taught wherein the source address and the destination address in the memory correspond to 16 bit or 8 bit memory locations. However, it as been held that change in size is not a patentable difference, *In re Rose, 105 USPQ 237 (CCPA 1955).* Any sizes of the source and destination memory locations are not patentably distinct over the prior art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the source address and the destination address in the memory correspond to any size of memory location, including 16 and 8 bits, as it has been held that changes in size is not a patentable difference *In re Rose, 105 USPQ 237 (CCPA 1955).*

15. Referring to claim 8, Intel has taught the method of claim 1, as described above, and wherein the accessing the first operand further comprises, calculating the source address in the

memory from data in the 11 bits of the 32-bit instruction specifying a source address in a memory (Inherent).

16. Referring to claim 9, Intel has taught the method of claim 8, as described above. The cited portion of Intel has not specifically wherein calculating comprises using one address mode of the group consisting of a Register + Immediate, a Register + Register Indirect, a Register + Immediate Auto-Increment, a Register Direct, and an Immediate addressing mode. However, Official Notice is taken that Register + Immediate, a Register + Register Indirect, a Register + Immediate Auto-Increment, a Register Direct, and an Immediate addressing modes are well known in the art for calculating a source address in a memory. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to calculate using one address mode of the group consisting of a Register + Immediate, a Register + Register Indirect, a Register + Immediate Auto-Increment, a Register Direct, and an Immediate addressing mode, as these are well known addressing modes for sour! ce address calculation.

17. Claim 10 is rejected for the same reasons as set forth in claim 1.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, 1995 (herein after Intel), in view of Case et al., US Patent 4,777,587 and Suzuki et al., US Patent 5,907,694 (herein after Suzuki).

19. Referring to claim 4, Intel and Case have taught the method of claim 1,as described above. Intel has not specifically taught further comprising the step of passing through a sign extender the first operand in response to the source address corresponding to a memory location of less than 32 bits. However, Suzuki et al. have taught the step of passing through a sign

extender a first operand in response to a source address corresponding to a memory location of less than the size of the woriking registers, for the desirable purpose of accomodating the data in a register (abstract, Figure 2, elemwnt 16, column 2, line 33-column 6, line 62). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to pass the first operand of Intel through a sign extender, as taught by Suzuki et al., in response to the source address corresponding to a memory location of less than 32 bits, for the desirable purpose of accommodating the source into a working Intel register.

20. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, 1995 (herein after Intel), in view of Case et al., US Patent 4,777,587, Suzuki et al., US Patent 5,907,694 (herein after Suzuki), and Langdon, Jr., US Patent 4,110,831 (herein after Langdon). Intel has taught the method of claim 4, as described above. Intel has not specifically taught further comprising truncating the result prior to storing it in the destination address in the memory. However, Langdon has taught truncating a result prior to storing in an address in memory for the desirable purpose of maintaining the most significant bits of result while discarding the insignificant bits that would otherwise overflow the memory (column 5, line 35-column 6, line 67). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to truncate the result of Intel prior to storing in the destination address in the memory, as taught by Langdon, for the desirable purpose of maintaining the most significant bits of the result while discarding the insignificant bits that would otherwise overflow the memory.

21. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel

Corporation, Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, 1995 (herein after Intel), in view of Case et al., US Patent 4,777,587 (herein after Case) and Kurakazu et al., US Patent 4,825,355 (herein after Kurakazu).

22. Referring to claim 6, Intel has taught the method of claim 1, as described above. Intel has not specifically taught wherein the instruction specifies a size of the first operand, the size being one of 8 bits, 16 bits, and 32 bits. However, Kurakazu has taught an instruction that specifies the size of a first operand being one of 8 bits, 16 bits, and 32 bits (Kurakazu, abstract, Figures 1A-B and 2, column 1, lines 21-25 and 60-67, column 2, lines 44-66) for the desirable purpose of avoiding the need to modify the bit length of the operand and consequently speed up program execution. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instruction of Intel specify the size of a first operand being one of 8 bits, 16 bits, and 32 bits, as taught by Kurakazu, for the desirable purpose of avoiding the need to modify the bit length of the operand and consequently speeding up program execution (Kurakazu, abstract, Figures 1A-B and 2, column 1, lines 21-25 and 60-67, column 2, lines 44-66).

23. Referring to claim 7, Intel in combination with Case and Kurakazu have taught the method of claim 6, as described above, and wherein the size of the first operand is specified in an operation code within the 5 bits of the mathematical operation to be performed (Kurakazu, abstract, Figures 1A-B and 2, column 1, lines 21-25 and 60-67, column 2, lines 44-66).

Response to Arguments

24. Applicant's arguments have been fully considered but they are not persuasive.

25. On page 14, Applicant argues in essence:

"The reference does not show both a source and a destination address in the memory that are not the same. ... Since the result is assigned to the first operand, there is not need to specify an additional memory address, as the claim requires."

However, it is respectfully pointed out that the claims do not require both a source and a destination address in the memory that are not the same. If applicant would like specific limitations read into the claims, then Applicant should specifically claim those limitations. Therefore this argument is moot.

26. On pages 14 and 15, Applicant argues in essence:

"The Intel reference describes that its two-operand instructions, such as the ADD instruction, are not memory to memory and that memory to memory data transfers cannot be accomplished directly as claim 1 recites but rather indirectly either implicitly through a memory-based stack or using the registers..."

However, Intel has in fact taught a memory-to-memory ADD instruction. When DEST is a memory location, SRC must be a register (This is supported by 3-18 cited by applicant.). In this case, a value at a memory location DEST is added to a register value SRC and the result is stored back in a memory at location DEST. An instruction that adds a value from a register and a memory and stores the result in memory is necessarily a memory-to-memory instruction. Therefore this argument is moot.

27. On page 15, Applicant argues in essence:

"The Case fails to show or suggest the use of (1) "a source address in a memory," (2) "A source address in a register file," and (3) "a destination address in the memory" as recited in claim 1."

However, Case has not been cited for having taught the use of (1) "a source address in a memory," (2) "A source address in a register file," and (3) "a destination address in the memory" as recited in claim 1. Intel has been taught for teaching the limitations in

question. See the rejection to claim 1 above. Therefore this argument is moot.

28. On page 17, Applicant argues in essence:

"In support of the combination, Examiner contends that "a person in the art would have been motivated to combine the cited references because of the desirable purpose of simplifying instruction decoding." In order to support a rejection under 35 USC 103, however the Examiner must provide "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine. The Examiner has not cited an objective prior art reference that provides an incentive, motivation, or suggestion for making the suggested combination. Also, Examiner has not established by objective evidence that knowledge generally available to one of ordinary skill in the art would lead one to make the suggested combination. Thus, Applicant's respectfully assert that the suggested combination is improper. "!

However, it is extremely well known in the art that fixed length instructions are much simpler to decode then variable length instructions. To further support this assertion, Applicant is respectfully directed to Mahalingaiah, US Patent 6,460,116, column 1, line 57-column 2, line 46, column 3, lines 41-45. Therefore the rejection is proper and this argument is moot.

Allowable Subject Matter

29. Claims 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

30. Claims 11-15 and 18 are allowed.

Conclusion

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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